# 20EC21P5 - VHDL PROGRAMMING LABORATORY

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| Course Category: | Program Core | Credits: | 1.5 |
| Course Type: | Practical | Lecture-Tutorial-Practical: | 0-0-3 |
| Prerequisite: | Knowledge on VHDL programming for to design basic logic gates, combinational circuits and flip-flops. | Sessional Evaluation:Univ. Exam Evaluation:Total Marks: | 4060100 |
| Objectives: | * To learn the VHDL programming constructs and its implementation
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| Course Outcomes | Upon successful completion of the course, the students will be able to Solve problems using VHDL programming concepts |
| Course Content | 1. To implement AND, OR and NOT logic gates.
2. To implement NAND, NOR, EX-OR AND EX-NOR logic gates
3. To implement half adder and full adder.
4. To implement half subtractor and full subtractor.
5. To implement binary to gray and gray to binary code converters.
6. To implement BCD to 7 segment displayers
7. To implement magnitude comparator.
8. To implement decoder and encoder.
9. To implement multiplexer and demultiplexer.
10. To implement SR flip-flop
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| Text Books &ReferencesBooks | **TEXT BOOKS:**1. Digital Design with an introduction to the Verilog HDL, VHDL and system verilog 6th edition by M.Morris Mano Michael D.Ciletti

**REFERENCE BOOKS:**1. Fundamentals of Digital Circuits fourth edition A.Ananda Kumar,
2. A VHDL Primer 3rd edition by J Bhaskar
3. Very log HDL a guide to Digital Design and Synthesis by Samir Palnitkar
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| E-Resources | 1. <https://nptel.ac.in/courses>
2. <https://freevideolectures.com/university/iitm>
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**CO-PO Mapping:** 3-High Mapping, 2-Moderate Mapping, 1-Low Mapping, - -Not Mapping

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|   | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** | **PSO1** | **PSO2** | **PSO3** |
| **CO1** | - | 3 | - | - | - | 1 | - | - | - | - | - | - | 3 | 2 | 1 |